The system of the invention also includes capacitor/readout units for transferring, multiple times, charge from the detector to the capacitor and back. In embodiments discussed in the specification, a plurality of transfer and readout capacitors is provided for multiple readouts. Readout noise can be reduced by reading out a single CCD element multiple times and averaging the results.

As discussed in the specification, a light detector collects light during the duration of a light collection period, sometimes referred to as a pixel. Thereafter, charges transferred to a readout capacitor and the voltage across that capacitor can then be sampled. Since there is finite transfer noise, multiple transfers result in different numbers of electrons in the readout capacitor and thus result in different voltages. By transferring the charge into and out of the readout capacitor multiple times, and by averaging the readings, one can diminish the impact of this readout noise by a significant amount.

In the Office Action, the Examiner has objected to the drawings requiring details of the capacitor/readout units to be added. In response, Figs. 3 and 4 are being amended as shown in red on the accompanying pages to comply with the Examiner's request. As now shown in Figs. 3 and 4, each of the capacitor/readout units includes a capacitor and standard circuitry for sampling the voltage across the capacitor. It is submitted that these amendments comply with the Examiner's request. The specification is also being amended to be consistent with amended Figs. 3 and 4. It is further submitted that no new matter is being introduced in that there is clear support in the specification. For example, beginning on the last line of page 2 and continuing at the beginning of page 3, the specification states: "After that period, its charge is transferred to a readout capacitor and the voltage across that capacitor can then be sampled." Figs. 3 and 4 as now amended explicitly illustrate the capacitors and their being read out by standard circuitry.

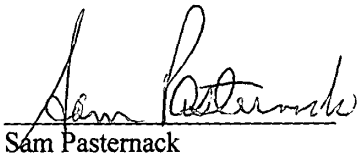
Claims 1-3, and 6 stand rejected under 35 USC §102(b) as being anticipated by Kamasz, et al. With respect to claim 1, the Examiner indicates that Kamasz discloses a detector system with means for generating a light beam having an area and a detector with a cell size comparable to the light beam area. The Examiner refers to laser pulses at column 6, lines 13, 14 and refers to Fig. 3A. Kamasz, et al. deals with light detectors in which background illumination is reduced by a subtraction technique. With respect to Fig. 3A and the description related thereto, it is submitted that there is no teaching of providing a detector having a cell size comparable to a light beam area. The specification is entirely silent as to the relationship between light detector

area and beam area. The Examiner's attention is directed to Fig. 2 which clearly shows that spot 210 is much smaller than the area of pixel 214. Thus, Kamasz, et al. does not anticipate claim 1. Dependent claims 2, 3, and 6 depend from claim 1 and are allowable over Kamasz, et al. for the reasons set forth with respect to independent claim 1.

Claims 4, 5, 7, and 8 stand rejected under 35 USC §103(a) as being unpatentable over Kamasz, et al. These claims are directed to the high quantum efficiency point detector system that further includes a readout capacitor and means for transferring, multiple times charge from the detector to the capacitor. There may be a plurality of transfer and readout capacitors arranged in a pipeline configuration or arranged in a cyclic pattern around a light sensitive area. It is submitted that there is no teaching or suggestion whatsoever in Kamasz, et al. that would meet the limitations in claims 4, 5, 7, and 8. It appears that the Examiner is making an impermissible hindsight reconstruction in this regard. Reconsideration is requested.

For the foregoing reasons, it is submitted that the pending claims are allowable over Kamasz, et al. and early favorable action is requested.

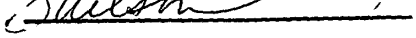
Respectfully submitted,



Sam Pasternack
Registration No.: 29,576

AGILENT TECHNOLOGIES, INC.
Intellectual Property Administration, LE
P. O. Box 7599
M/S DL 429
Loveland, Colorado 80537-0599
Dated: September 24, 2002

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner For Patents, Washington, D.C. 20231
on 9-24-02



MARKED-UP VERSION SHOWING CHANGES

Specification, page 3, line 20:

- If multiple capacitors are used for charge to be stored in and read out from while subsequent charge collection processes are in progress, these capacitors may be arranged in a pipeline fashion as shown in Fig. 3. A first charge is generated in a light-sensitive area 30 and then moved to a first capacitor/readout unit 31. The capacitor/readout unit 31 includes a capacitor 31a and a voltage sampling circuitry 31b for sampling the voltage across the capacitor 31a. While a second charge is generated in the light-sensitive area 30, the first charge is read out and cycled back as often as desired. Once the second charge has been generated, the first charge is either dumped or moved into a second capacitor/readout unit 32, while the second charge is moved to the first capacitor/readout unit 31 after which a third charge can be generated in the photo-sensitive area 30. The capacitor/readout unit 32, like the capacitor/readout unit 31, includes a capacitor 32a and circuitry 32b for sampling the voltage across the capacitor 32a. All readings of a given charge taken from different capacitors are averaged to reduce the noise on the charge measurement. This process can be extended in a similar fashion to a large number of capacitors (32 through 33), thus reducing readout noise. As will be appreciated, the capacitor/readout unit 33 includes a capacitor 33a and circuitry 33b to sample the voltage across the capacitor 33a. In this design, any given charge is essentially moved along a line of capacitors to allow it to be read out as often as desired. After all desired readout/averaging is done, the charge is dumped (as in a conventional CCD). –

Specification, page 4, line 5:

-- In an alternate design shown in Fig. 4, there are several (in this case four) capacitors with associated readout circuitry arranged around the light-sensitive area 30. Charge from individual charge generation cycles (pixel times) is transferred to these capacitors, e.g., cycling around. A first charge is moved to capacitor/readout unit 35 and stays there for four pixel cycles for repeated readout. The capacitor/readout unit 35 includes a capacitor 35a and circuitry 35b for

sampling the voltage across the capacitor 35a. One pixel cycle later the next charge is moved to capacitor/readout unit 36, another cycle later the next charge is moved to capacitor/readout unit 37. It will be appreciated that the capacitor/readout unit 36 includes a capacitor 36a and circuitry 36b to sample the voltage across the capacitor 36a. Similarly, the capacitor/readout unit 37 includes a capacitor 37a along with circuitry 37b to sample its voltage. The next charge generated is moved to capacitor/readout unit 38 which includes a capacitor 38a and circuitry 38b to sample its voltage. Once the next charge is generated, the charge in capacitor/readout unit 35 is dumped and the new charge is moved there, thus restarting the cyclic acquisition of the data. --